FreeRTOS

…What's new in the FreeRTOS project

Richard Barry
Founder, FreeRTOS Project
Principal Engineer, AWS IoT

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Agenda

The FreeRTOS Kernel

Amazon FreeRTOS

New Ecosystem Projects

New Architecture Ports

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FreeRTOS—Open source real time kernel

is everywhere…

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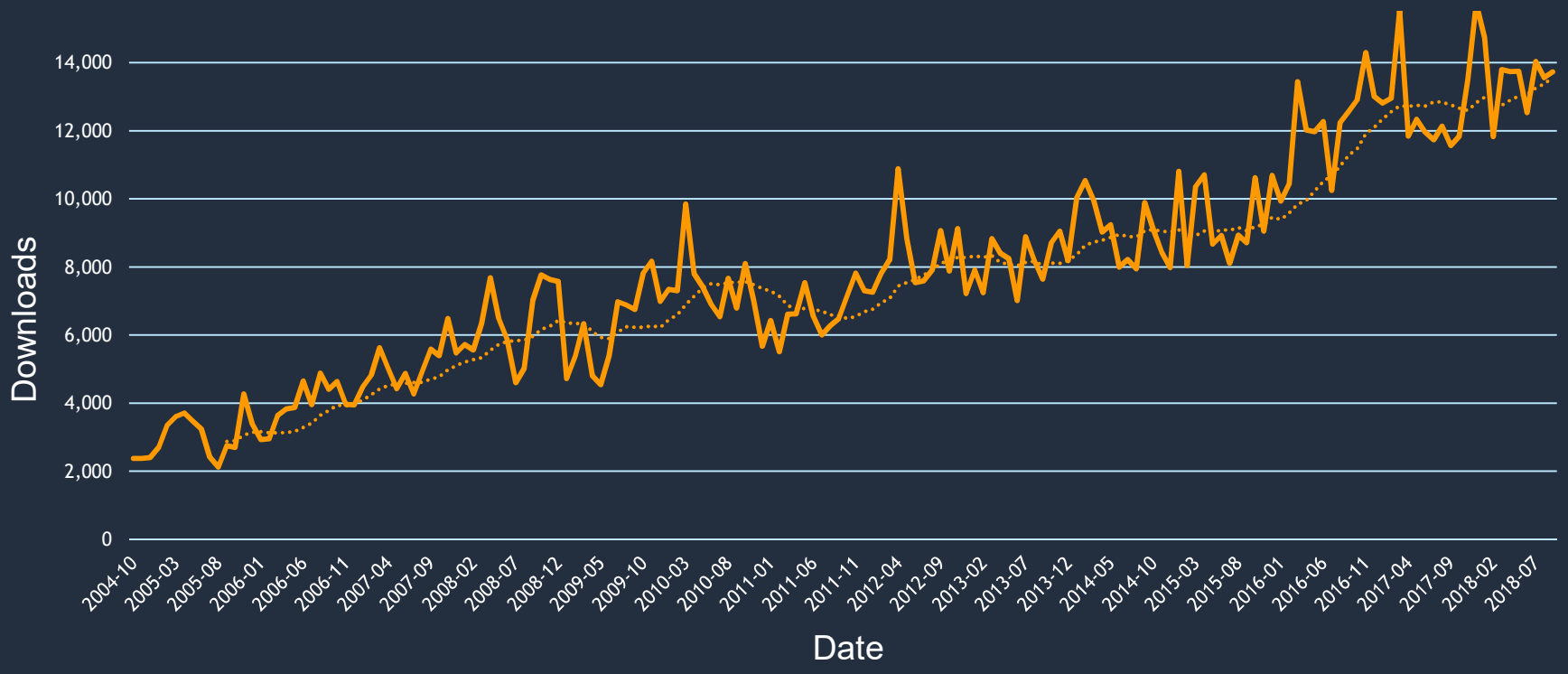
FreeRTOS downloads per month over 15 years



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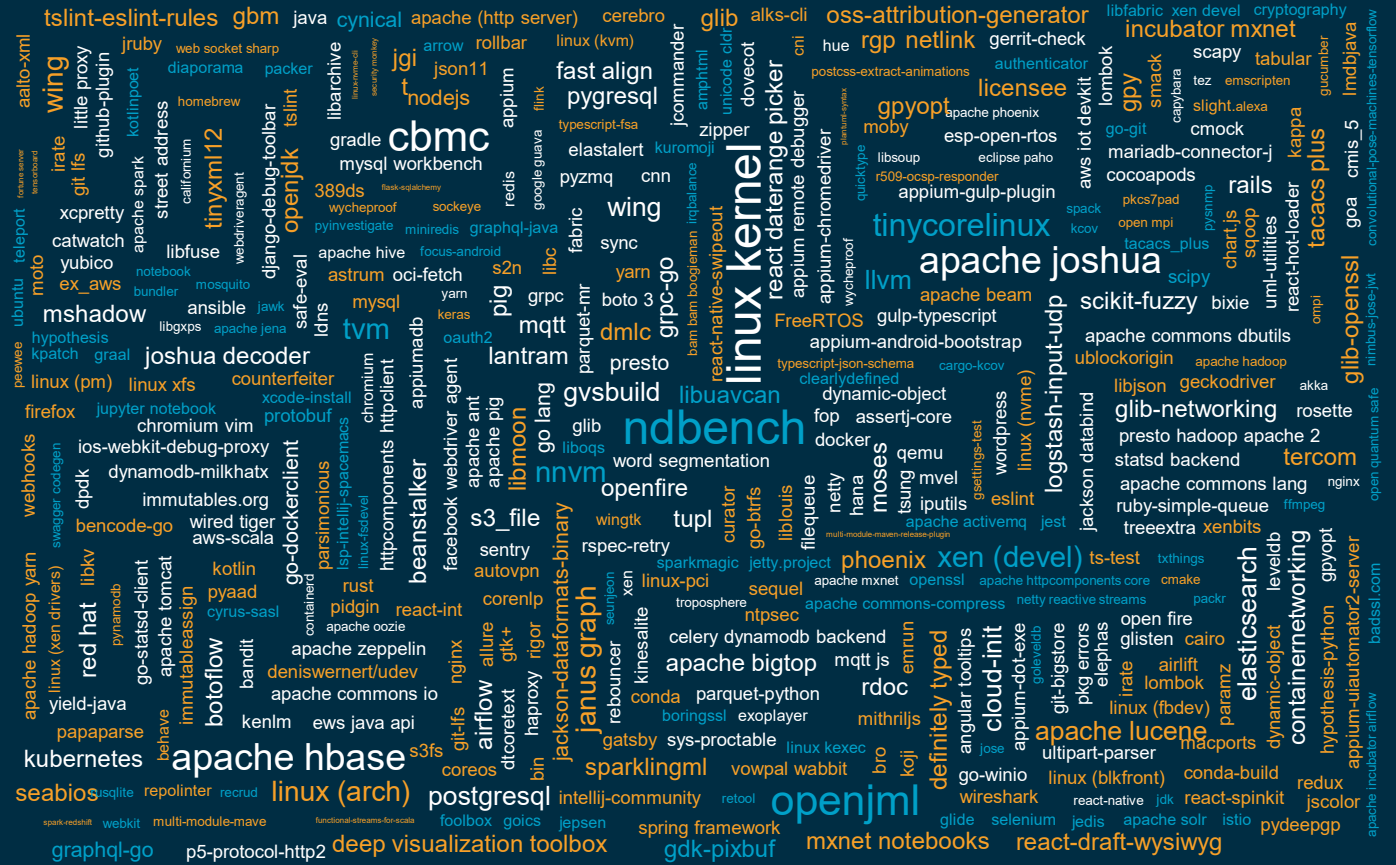
2018

2017

2016



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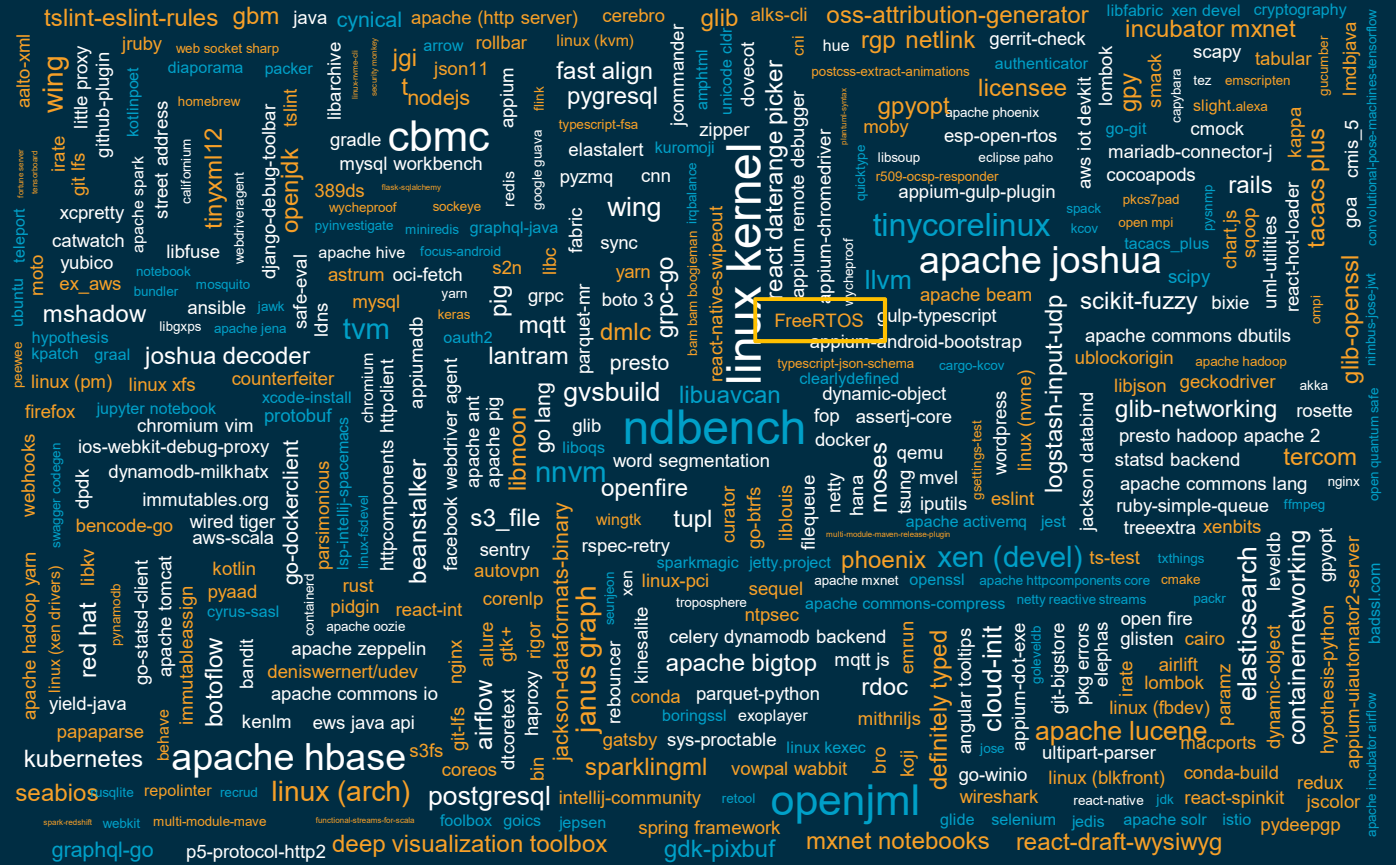
2018

2017

2016



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Use Cases

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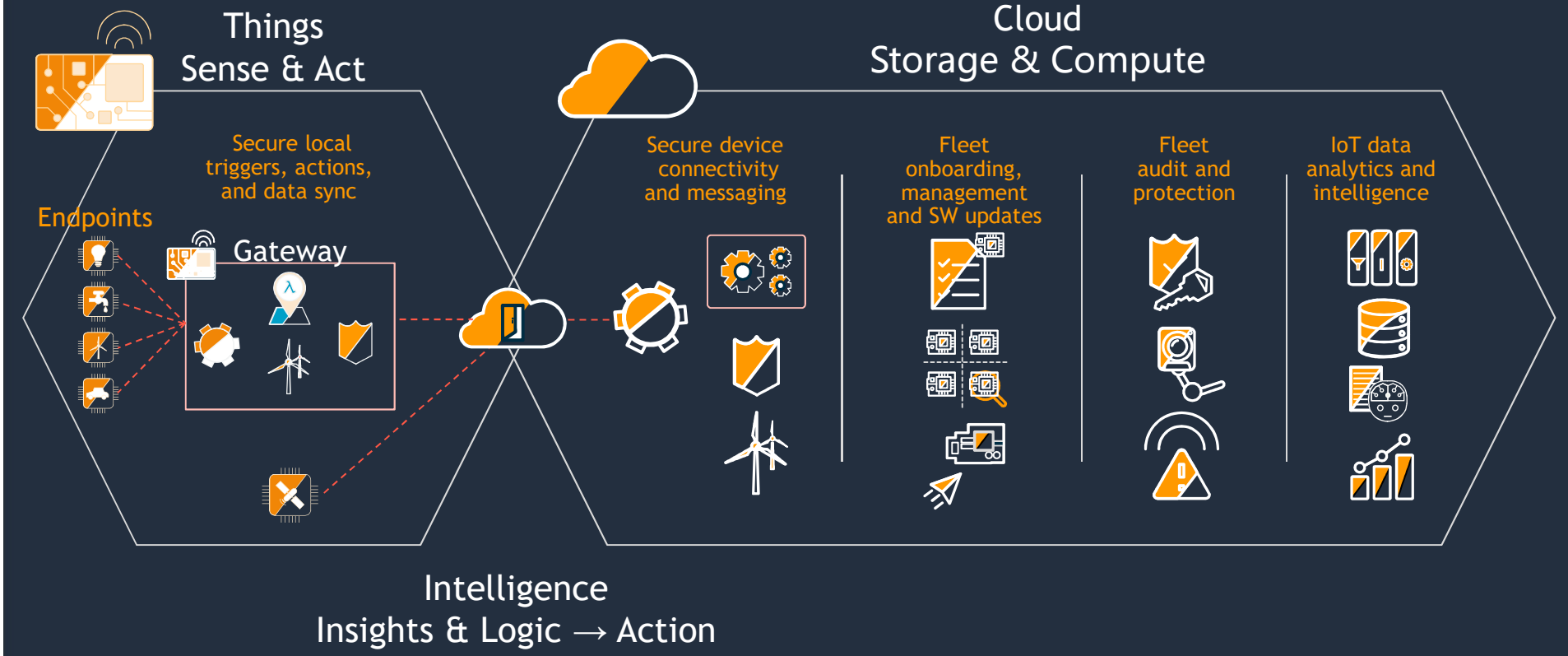
Amazon FreeRTOS



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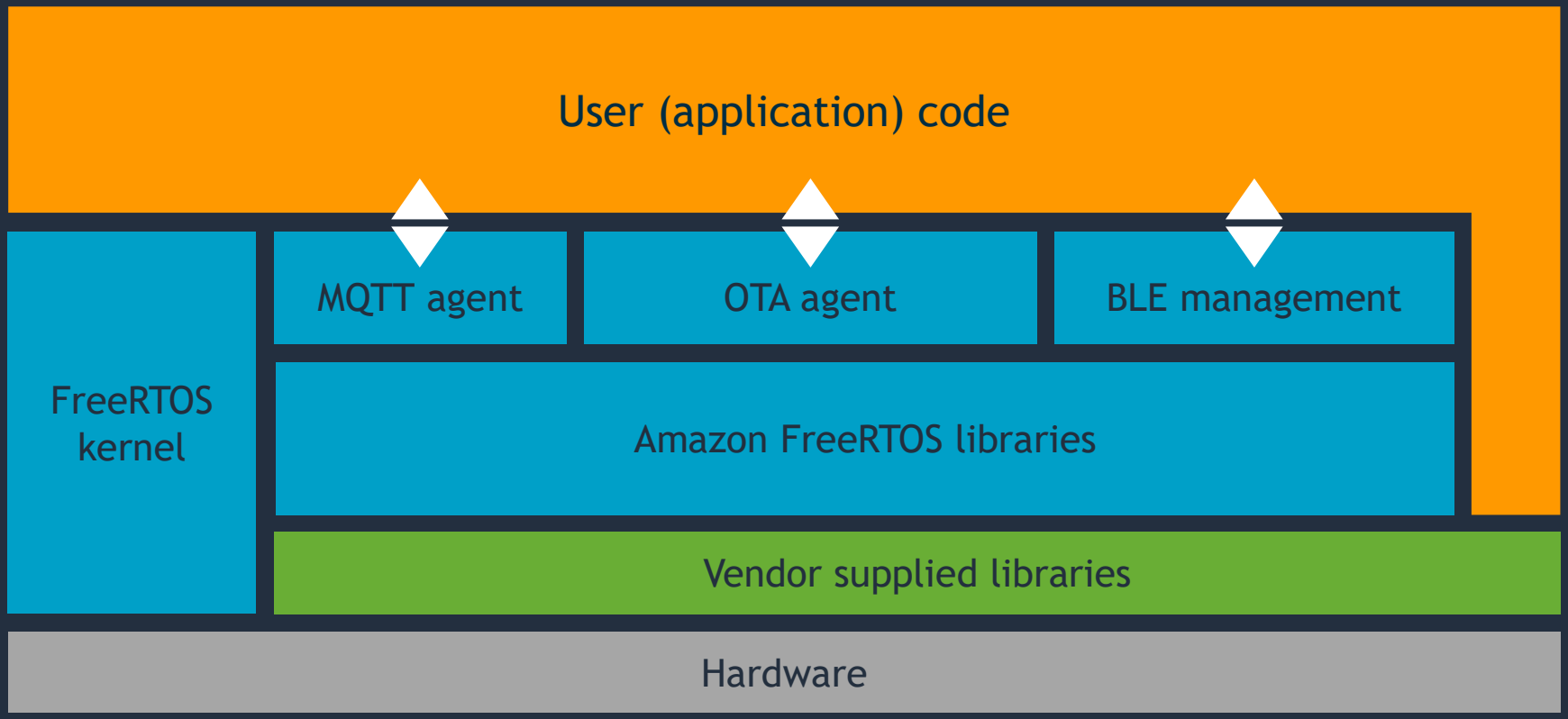
Amazon FreeRTOS



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New Ecosystem Products

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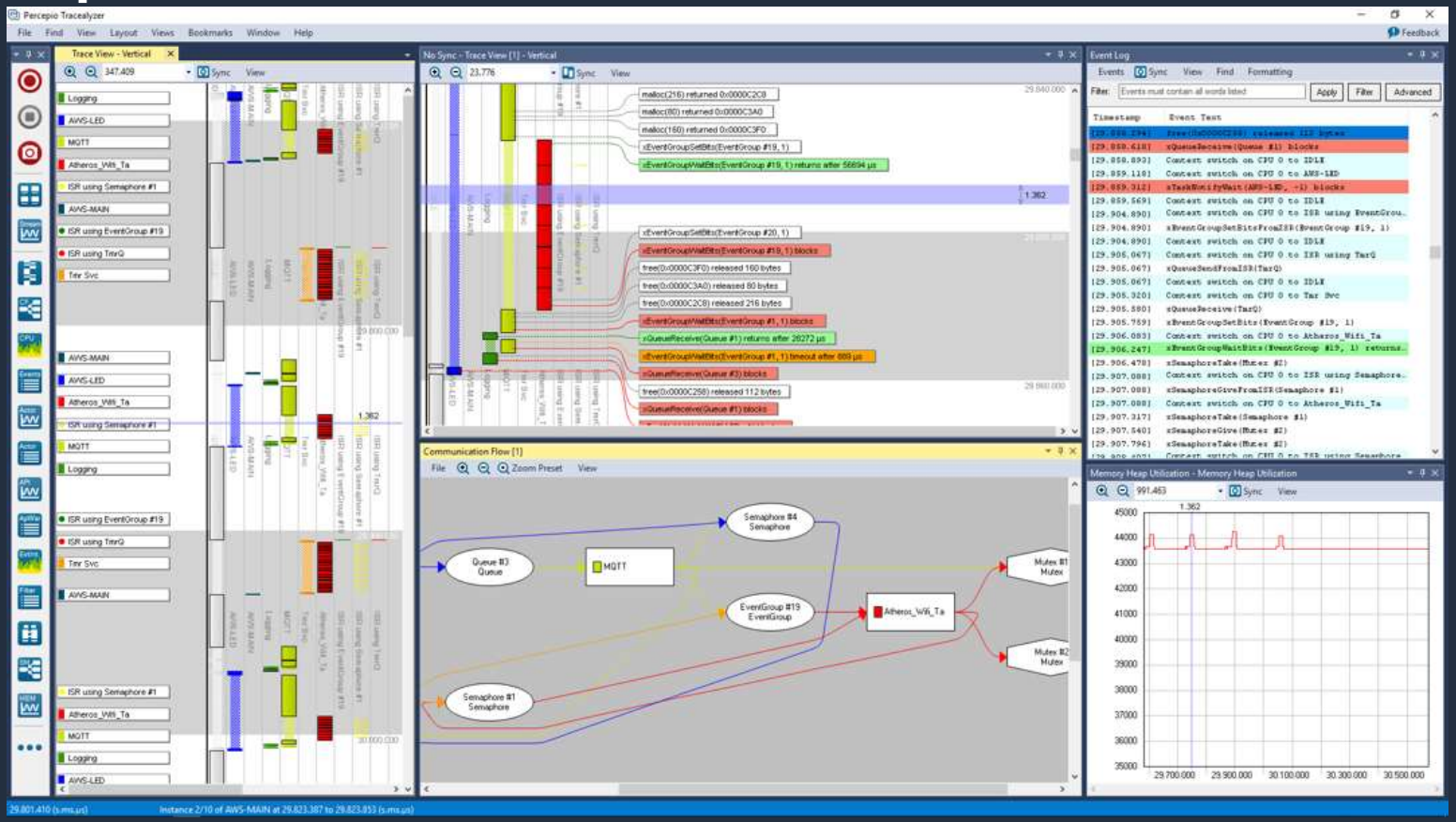
Percepio Device Firmware Monitor ™



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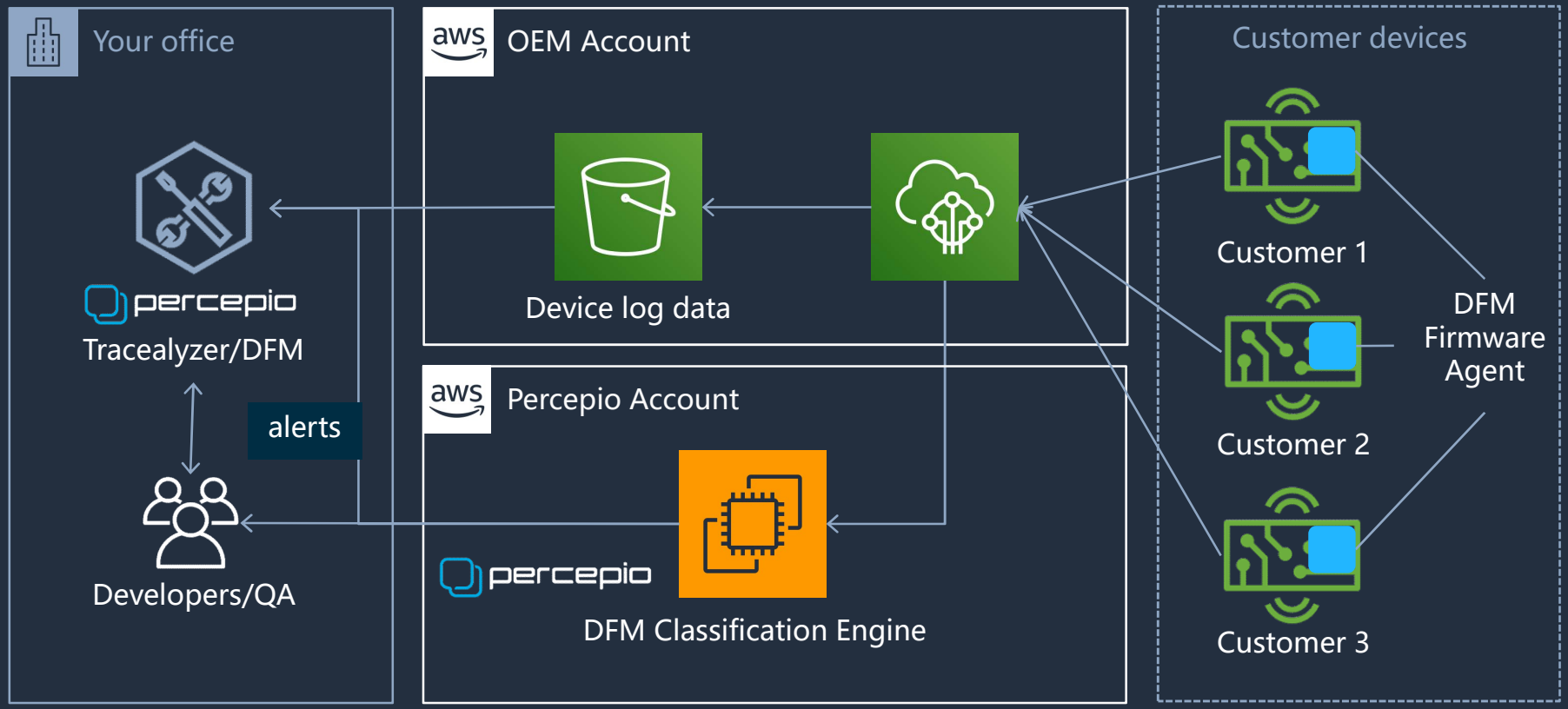
Percepio Device Firmware Monitor ™



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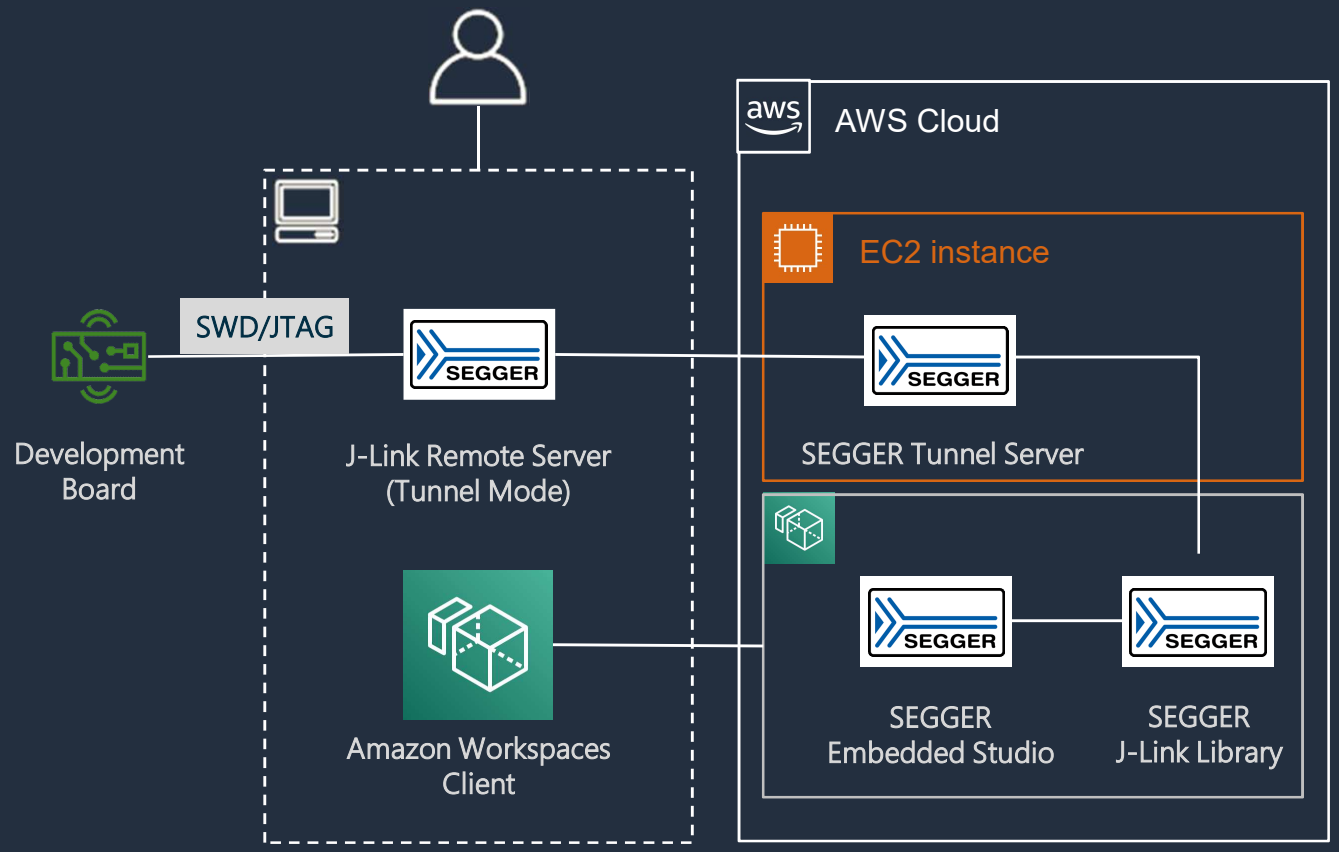
SEGGER Driven Remote Development



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New Architecture Ports

FreeRTOS Kernel V10.2.0

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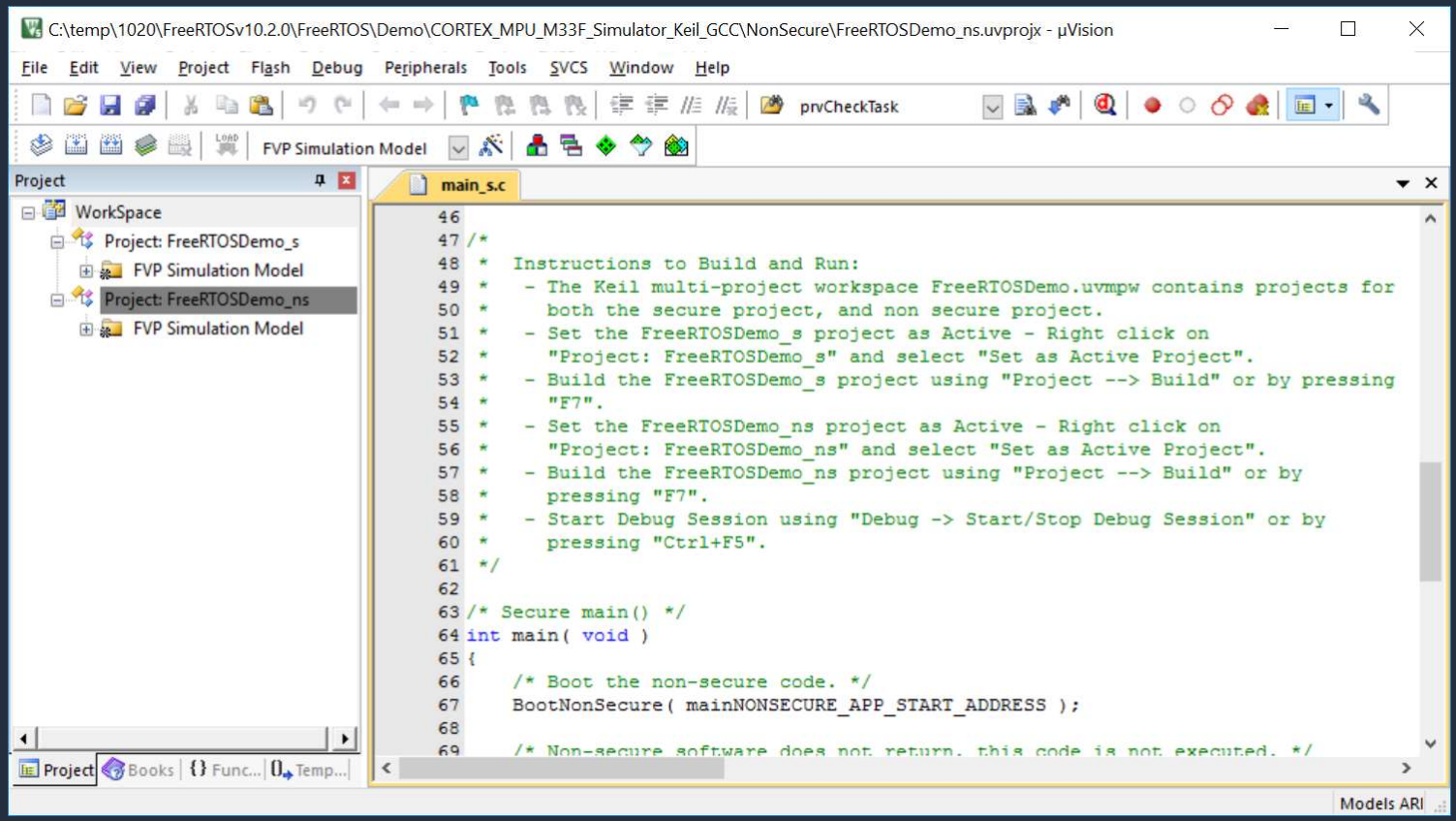
ARMv8-M (Cortex-M33)



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RISC-V

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RISC-V ISA & Foundation Overview

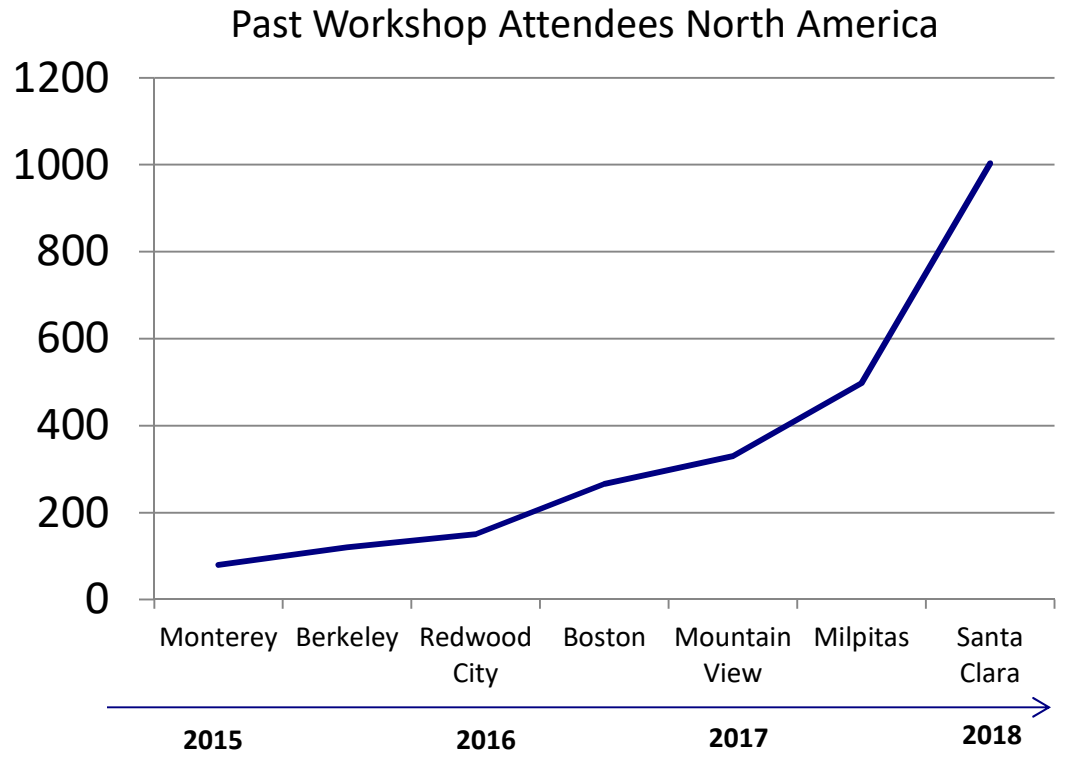
Rick O'Connor, Executive Director
rickoco@riscv.org
http://www.riscv.org

RISC-V Ecosystem Growth

Dec 2018 Summit / Ecosystem Growth

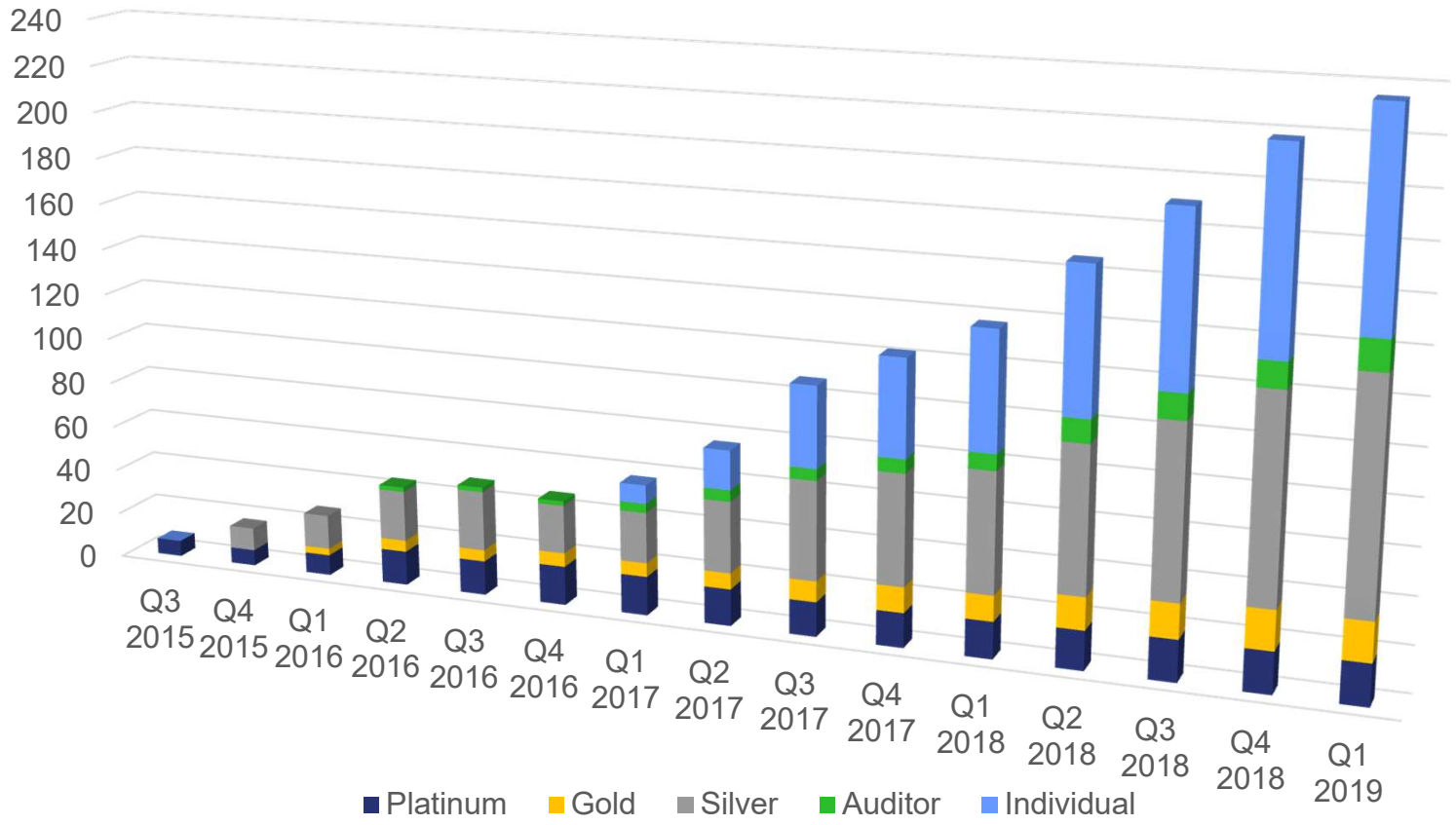
RISC-V Summit Dec 2018

- over **1000** registered attendees
- **~ 2X** the attendance of the Milpitas Workshop in Dec 2017
- **~ 250** abstracts submitted
- **59** sessions including keynotes, tutorials and 3 tracks
- **29** exhibitors



RISC-V Foundation Growth History

September 2015 to February 2019



Berkeley Architecture Research
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antmicro
SANECHIPS 中兴微电子
Western Digital.
NVIDIA.
bluespec
ORION 猎户星空
SAMSUNG
Google
QUALCOMM
THALES
Micron
MICROCHIP
C-SKY 中天微
cortus
Rambus
SiFive
MARVELL
RISC-V®
Foundation: 200+ Members
ESPRESSIF
MEDIATEK
HiGo 海高
QuickLogic
ANDES TECHNOLOGY
galois
imperas
REM
oculus
BAE SYSTEMS
Esperanto TECHNOLOGIES
NUS
Inria
inside secure
Hortonworks
सी डैक CDAC
ETH zürich
SECURE RF
Symbiotic EDA
Hewlett Packard Enterprise
TIMESILICON
VeriSilicon
SK hynix
OpenSingularity
INTRINSIC ID
MIT CSAIL
Honeywell THE POWER OF CONNECTED
Barcelona Supercomputing Center Centro Nacional de Supercomputación
BSC
SIEMENS
Baylibre
TRINAMIC MOTION CONTROL
cea
GOWIN
INTRINSIX
Minima
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NORTHROP GRUMMAN
jumptrading
BOSTON UNIVERSITY
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君正 Ingenic
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astc
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DATA 61
CSIRO
GRAY RESEARCH
PEZY Computing
IBM
cadence
SoundAI
COBHAM
XtremeEDA
AdaCore
Alibaba Group 阿里巴巴集团
lowRISC
MOSIS
ultraSoC
Canaan
CMC MICROSYSTEMS
BITMAIN
GREENWAVES TECHNOLOGIES
SHC SH CONSULTING
APEXMIC
Syntacore Custom cores and tools
VectorBlox embedded supercomputing
SEAGATE
Technolution
EMDALO TECHNOLOGIES
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tsmc
0x5 HEX-Five Security
TCL Tactical Computing Labs
codasip
Rumble Development
csem
Roa Logic
aselsan
LATTICE SEMICONDUCTOR
BERKELEY LAB
PRINCETON UNIVERSITY
Aril Inc
Blockstream
dxcorr
TechanaLye
NERVOS
ALLWINNER
HUAWEI
expresslogic

So what's all the fuss about?

Its just an ISA right?

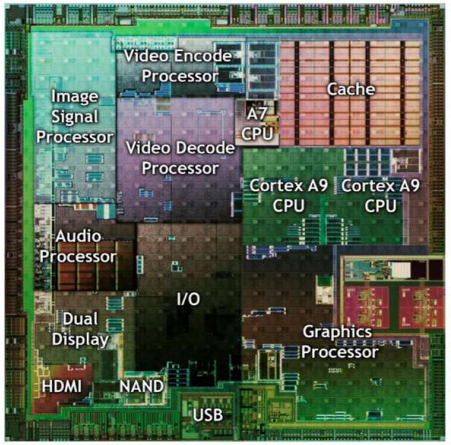
How did we get here?

RISC-V Background

- Started as a research project at UC Berkeley in 2010 and resulted in the release of the base user spec in May, 2014
  - many tapeouts and several research publications along the way
- The name RISC-V (pronounced *risk-five*), was chosen to represent the fifth major RISC ISA design effort at UC Berkeley
  - RISC-I, RISC-II, SOAR, and SPUR were the first four projects with the original RISC-I publications dating back to 1981
- In August 2015, articles of incorporation were filed to create a non-profit RISC-V Foundation to govern the ISA

Most CPU chips are SoCs with many ISAs

- Applications processor
- Graphics processors
- Image processors
- Radio DSPs
- Audio DSPs
- Security processors
- Power-management processor
- ….



NVIDIA Tegra SoC

- Apps processor ISA too large for base accelerator ISA
- IP bought from different places, each proprietary ISA
- Home-grown ISA cores
- Over a dozen ISAs on some SoCs – each with unique software stack

Why so Many ISAs?

Do we need all these different ISAs?

Must they be proprietary?

What if there was one free and open ISA everyone could use for everything?

What's Different about RISC-V?

- ***Simple***
  - Far smaller than other commercial ISAs
- ***Clean-slate design***
  - Clear separation between user and privileged ISA
  - Avoids µarchitecture or technology-dependent features
- A ***modular*** ISA
  - Small standard base ISA
  - Multiple standard extensions
- Designed for ***extensibility/specialization***
  - Variable-length instruction encoding
  - Vast opcode space available for instruction-set extensions
- ***Stable***
  - Base and standard extensions are frozen
  - Additions via optional extensions, not new versions

Summary

- The free and open RISC-V ISA is enabling a new innovation frontier across all computing devices
- Strong Industry Support
  - ~200+ members; Broad commercial and academic interest
- RISC-V Twitter http://twitter.com/risc_v @risc_v
- RISC-V LinkedIn Page
  - http://www.linkedin.com/company/risc-v-foundation
- RISC-V mail lists / groups
  - https://riscv.org/mailing-lists/

FreeRTOS on RISC-V

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RISC-V examples in FreeRTOS V10.2.0

Pre-configured examples:

- QEMU sifive_e model using Freedom Studio
- Microsemi/Future Electronics M2GL025-Creative-Board using SoftConsole
- VEGAboard using vanilla Eclipse (https://www.open-isa.org)

FreeRTOS RISC-V specifics:

- Including the source files
- Setting the assembler's include file
- Set configCLINT_BASE_ADDRESS
- #define portasmHANDLE_INTERRUPT
- Install the FreeRTOS trap hander

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Thank You!

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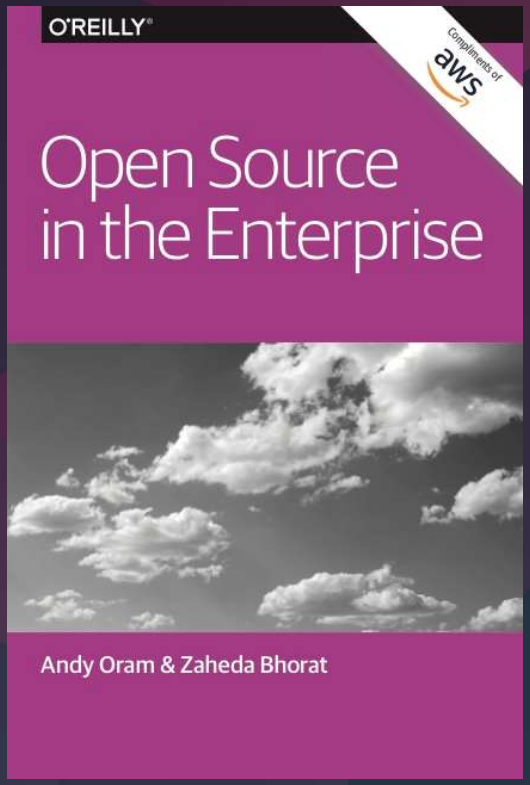

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